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PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

8291/8292 GPIB PERIPHERALS

December 1978

PRELIMINARY INFORMATION

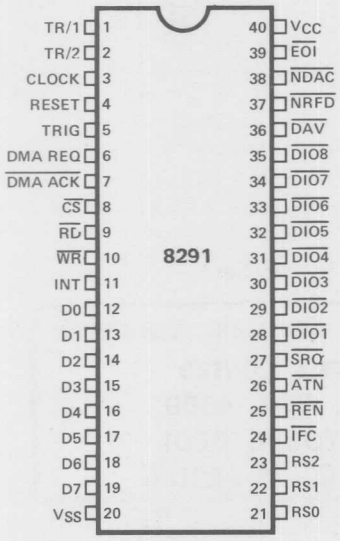
December 1978
9800542B

8291
GPIB TALKER/LISTENER

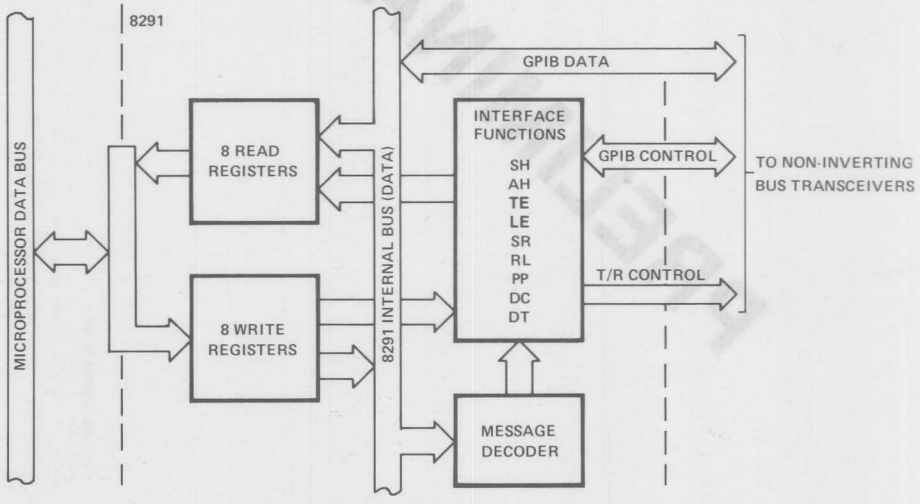
- Designed to Interface Microprocessors (e.g., 8080, 8085, 8086, 8048) to an IEEE Standard 488 Digital Interface Bus
- Programmable Data Transfer Rate
- Complete Source and Acceptor Handshake
- Complete Talker and Listener Functions with Extended Addressing
- Service Request, Parallel Poll, Device Clear, Device Trigger, Remote/Local Functions
- Selectable Interrupts
- On-Chip Primary and Secondary Address Recognition
- Automatic Handling of Addressing and Handshake Protocol
- Provision for Software Implementation of Additional Features
- 1 – 8 MHz Clock Range
- 16 Registers (8 Read, 8 Write), 2 for Data Transfer, the Rest for Interface Function Control, Status, etc.
- Directly Interfaces to External Non-Inverting Transceivers for Connection to the GPIB
- Provides Three Addressing Modes, Allowing the Chip to be Addressed Either as a Major or a Minor Talker/Listener with Primary or Secondary Addressing
- DMA Handshake Provision Allows for Bus Transfers without CPU Intervention
- Trigger Output Pin
- On-Chip EOS (End of Sequence) Message Recognition Facilitates Handling of Multi-Byte Transfers

The 8291 GPIB Talker/Listener is a microprocessor-controlled chip designed to interface microprocessors (e.g., 8048, 8080, 8085, 8086) to an IEEE Standard 488 Instrumentation Interface Bus. It implements all of the Standard's interface functions except for the controller.

PIN CONFIGURATION



BLOCK DIAGRAM

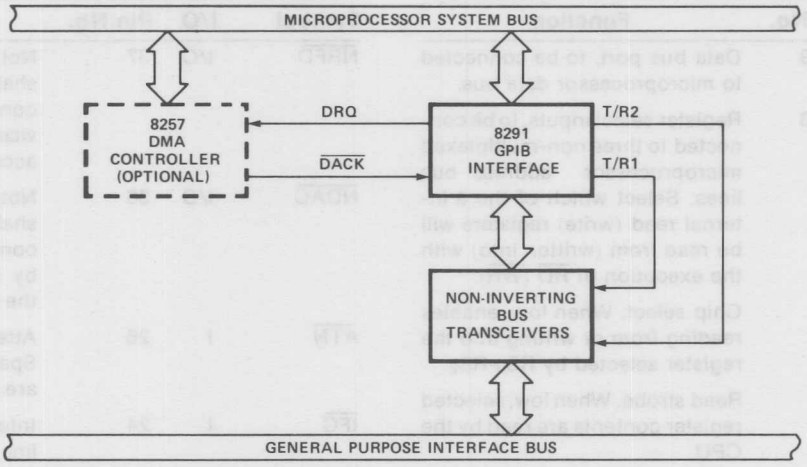


PIN DESCRIPTION

Symbol	I/O	Pin No.	Function
D_0-D_7	I/O	12-19	Data bus port, to be connected to microprocessor data bus.
RS_0-RS_2	I	21-23	Register select inputs, to be connected to three non-multiplexed microprocessor address bus lines. Select which of the 8 internal read (write) registers will be read from (written into) with the execution of $\overline{RD}$ ($\overline{WR}$).
$\overline{CS}$	I	8	Chip select. When low, enables reading from or writing into the register selected by RS_0-RS_2.
$\overline{RD}$	I	9	Read strobe. When low, selected register contents are read by the CPU.
$\overline{WR}$	I	10	Write strobe. When low, data is written into the selected register.
INT ($\overline{INT}$)	O	11	Interrupt request to the microprocessor, set high for request and cleared when the appropriate register is accessed by the CPU. May be software configured to be active low.
DMA REQ	O	6	DMA request, normally low, set high to indicate byte output or byte input, in DMA mode; reset by DMA ACK.
$\overline{DMA\ ACK}$	I	&	DMA acknowledge. When low, resets DMA REQ and selects data in/data out register for DMA data transfer (actual transfer done by $\overline{RD}$/$\overline{WR}$ pulse).
TRIG	O	5	Trigger output, normally low; generates a triggering pulse corresponding to the GET command.
CLOCK	I	3	External clock input, used for internal time delays generator. May be any speed in 1-8 MHz range.
RESET	I	4	Reset input. When high, forces the device into an "Idle" (initialization) mode. The device will remain at "Idle" until released by the microprocessor.
$\overline{DIO_1}$-$\overline{DIO_8}$	I/O	28-35	8-bit GPIB data port, used for bidirectional data byte transfer between 8291 and GPIB via non-inverting external line transceivers.
$\overline{DAV}$	I/O	36	Data valid; GPIB handshake control line. Indicates the availability and validity of information on the DIO lines.
$\overline{NRFD}$	I/O	37	Not ready for data; GPIB handshake control line. Indicates the condition of readiness of device(s) connected to the bus to accept data.
$\overline{NDAC}$	I/O	38	Not data accepted; GPIB handshake control line. Indicates the condition of acceptance of data by the device(s) connected to the bus.
$\overline{ATN}$	I	26	Attention; GPIB command line. Specifies how data on DIO lines are to be interpreted.
$\overline{IFC}$	I	24	Interface clear; GPIB command line. Places the interface functions in a known quiescent state.
$\overline{SRQ}$	O	27	Service request; GPIB command line. Indicates the need for attention and requests an interruption of the current sequence of events on the GPIB.
$\overline{REN}$	I	25	Remote enable; GPIB command line. Selects (in conjunction with other messages) remote or local control of the device.
$\overline{EOI}$	I/O	39	End or identify; GPIB command line. Indicates the end of a multiple byte transfer sequence or, in conjunction with ATN, addresses the device during a polling sequence.
T/R1	O	1	External transceivers control line. Set high to indicate output data/signals on the DIO_1-DIO_8 and DAV lines and input signals on the NRFD and NDAC lines (active source handshake). Set low to indicate input data/signals on the DIO_1-DIO_8 and DAV lines and output signals on the NRFD and NDAC lines (active acceptor handshake).
T/R2	O	2	External transceivers control line. Set high to indicate output signals on the EOI line. Set low to indicate expected input signal on the EOI line during parallel poll.
V_{CC}	P.S.	40	Positive power supply (5V ± 10%).
GND	P.S.	20	Potential ground circuit.

Note: all signals on the 8291 pins are specified with positive logic. However, IEEE 488 specifies negative logic on its 16 signal lines.

8291 SYSTEM DIAGRAM



THE GENERAL PURPOSE INTERFACE BUS (GPIB)

The General Purpose Interface Bus (GPIB) is defined in the IEEE Standard 488-1975 "Digital Interface for Programmable Instrumentation." Although a knowledge of this standard is assumed, Figure 1 provides the bus structure for quick reference. Also, Tables 1 and 2 reference the interface state mnemonics and the interface messages respectively. Modified state diagrams for the 8291 are presented in Appendix A.

GENERAL DESCRIPTION

The 8291 is a microprocessor controlled device designed to interface microprocessors e.g., 8048, 8080, 8085, 8086 to the GPIB. It implements all of the interface functions defined in the IEEE 488 Standard. If an implementation of the Standard's Controller function is desired, it can be connected with an Intel® 8292 to form a complete interface.

The 8291 handles communication between a microprocessor controlled device and the GPIB. Its capabilities include data transfer, handshake protocol, talker/listener addressing procedures, device clearing and triggering, service request, and both serial and parallel polling schemes. In most procedures, it does not disturb the microprocessor unless a byte is waiting on input or a byte sent on output (output buffer empty).

The 8291 architecture includes 16 registers. Eight of these registers may be written into by the microprocessor. The other eight registers may be read by the microprocessor. One each of these read and write registers is for direct data transfers. The rest of the write registers control the various features of the chip, while the rest of the read registers provide the microprocessor with a monitor of GPIB states, various bus conditions, and device conditions.

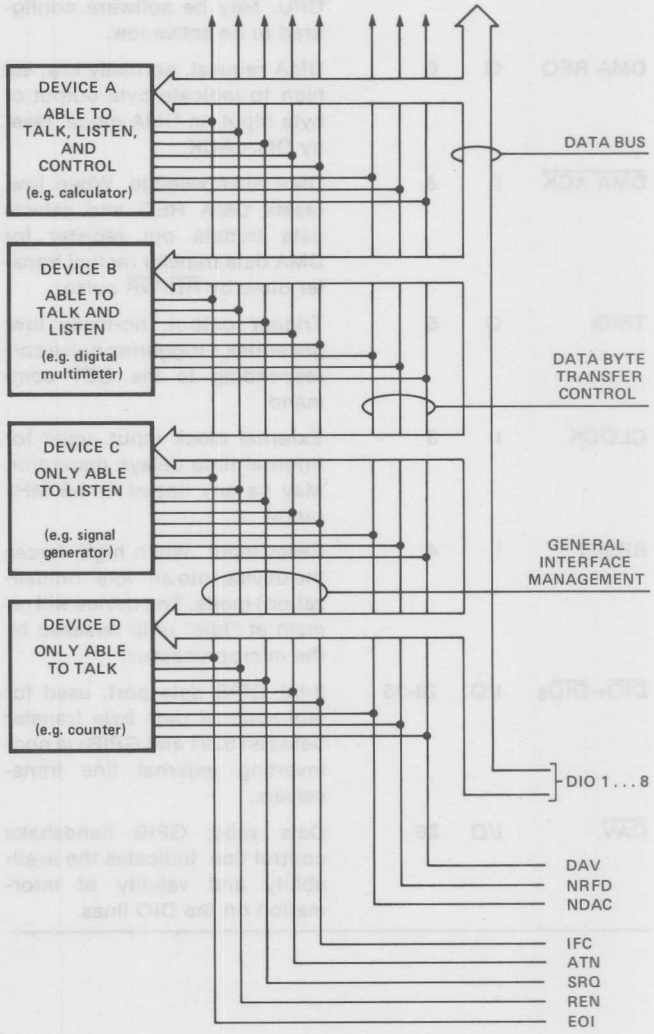


Figure 1. Interface Capabilities and Bus Structure.

GPIB Addressing

Each device connected to the GPIB must have at least one address whereby the controller device in charge of the bus can configure it to talk, listen, or send status. An 8291 implementation of the GPIB offers the user three addressing modes from which the device can be initialized for each application. The first of these modes allows for the device to have two separate primary addresses. The second mode allows the user to implement a single talker/listener with a two byte address (primary address + secondary address). The third mode again allows for two distinct addresses but in this instance, they can each have a two-byte address. However, this mode requires that the secondary addresses be passed to the microprocessor for verification. These three addressing schemes are described in more detail in the discussion of the Address registers.

TABLE 1.
IEEE 488 INTERFACE STATE MNEMONICS

Mnemonic	State Represented
ACDS	Accept Data State
ACRS	Acceptor Ready State
AIDS	Acceptor Idle State
ANRS	Acceptor Not Ready State
APRS	Affirmative Poll Response State
AWNS	Acceptor Wait for New Cycle State
CACS	Controller Active State
CADS	Controller Addressed State
CAWS	Controller Active Wait State
CIDS	Controller Idle State
CPPS	Controller Parallel Poll State
CPWS	Controller Parallel Poll Wait State
CSBS	Controller Standby State
CSNS	Controller Service Not Requested State
CSRS	Controller Service Requested State
CSWS	Controller Synchronous Wait State
CTRS	Controller Transfer State
DCAS	Device Clear Active State
DCIS	Device Clear Idle State
DTAS	Device Trigger Active State
DTIS	Device Trigger Idle State
LACS	Listener Active State
LADS	Listener Addressed State
LIDS	Listener Idle State
LOCS	Local State
LPAS	Listener Primary Addressed State
LPIS	Listener Primary Idle State
LWLS	Local With Lockout State
NPRS	Negative Poll Response State

Mnemonic	State Represented
PACS	Parallel Poll Addressed to Configure State
PPAS	Parallel Poll Active State
PPIS	Parallel Poll Idle State
PPSS	Parallel Poll Standby State
PUCS	Parallel Poll Unaddressed to Configure State
REMS	Remote State
RWLS	Remote With Lockout State
SACS	System Control Active State
SDYS	Source Delay State
SGNS	Source Generate State
SIAS	System Control Interface Clear Active State
SIDS	Source Idle State
SIIS	System Control Interface Clear Idle State
SINS	System Control Interface Clear Not Active State
SIWS	Source Idle Wait State
SNAS	System Control Not Active State
SPAS	Serial Poll Active State
SPIS	Serial Poll Idle State
SPMS	Serial Poll Mode State
SRAS	System Control Remote Enable Active State
SRIS	System Control Remote Enable Idle State
SRNS	System Control Remote Enable Not Active State
SRQS	Service Request State
STRS	Source Transfer State
SWNS	Source Wait for New Cycle State
TACS	Talker Active State
TADS	Talker Addressed State
TIDS	Talker Idle State
TPIS	Talker Primary Idle State

– – – – – – The Controller function is implemented on the Intel® 8292.

TABLE 2.
IEEE 488 INTERFACE MESSAGE REFERENCE LIST

Mnemonic	Message	Interface Function(s)
LOCAL MESSAGES RECEIVED (By Interface Functions)		
*gts	go to standby	C
ist	individual status	PP
lon	listen only	L, LE
lpe	local poll enable	PP
nba	new byte available	SH
pon	power on	SH,AH,T,TE,L,LE,SR,RL,PP,C
rdy	ready	AH
*rpp	request parallel poll	C
*rsc	request system control	C
rsv	request service	SR
rtl	return to local	RL
*sic	send interface clear	C
*sre	send remote enable	C
*tca	take control asynchronously	C
*tcs	take control synchronously	AH, C
ton	talk only	T, TE
REMOTE MESSAGES RECEIVED		
ATN	Attention	SH,AH,T,TE,L,LE,PP,C
DAB	Data Byte	(Via L, LE)
DAC	Data Accepted	SH
DAV	Data Valid	AH
DCL	Device Clear	DC
END	End	(via L, LE)
GET	Group Execute Trigger	DT
GTL	Go to Local	RL
IDY	Identify	L,LE,PP
IFC	Interface Clear	T,TE,L,LE,C
LLO	Local Lockout	RL
MLA	My Listen Address	L,LE,RL,T,TE
MSA	My Secondary Address	TE,LE,RL
MTA	My Talk Address	T,TE,L,LE
OSA	Other Secondary Address	TE
OTA	Other Talk Address	T, TE
PCG	Primary Command Group	TE,LE,PP
†PPC	Parallel Poll Configure	PP
†[PPD)	Parallel Poll Disable	PP
†[PPE]	Parallel Poll Enable	PP
*PPR_N	Parallel Poll Response N	(via C)
†PPU	Parallel Poll Unconfigure	PP
REN	Remote Enable	RL
RFD	Ready for Data	SH
RQS	Request Service	(via L, LE)
[SDC]	Select Device Clear	DC
SPD	Serial Poll Disable	T, TE
SPE	Serial Poll Enable	T, TE
*SQR	Service Request	(via C)
STB	Status Byte	(via L, LE)
*TCT or [TCT]	Take Control	C
UNL	Unlisten	L, LE

*These messages are handled only by Intel's 8292.
†Undefined commands which may be passed to the microprocessor.

TABLE 2. (Cont'd)
IEEE 488 INTERFACE MESSAGE REFERENCE LIST

Mnemonic	Message	** Interface Function(s)
REMOTE MESSAGES SENT		
ATN	Attention	C
DAB	Data Byte	(via T, TE)
DAC	Data Accepted	AH
DAV	Data Valid	SH
DCL	Device Clear	(via C)
END	End	(via T)
GET	Group Execute Trigger	(via C)
GTL	Go to Local	(via C)
IDY	Identify	C
IFC	Interface Clear	C
LLO	Local Lockout	(via C)
MLA or [MLA]	My Listen Address	(via C)
MSA or [MSA]	My Secondary Address	(via C)
MTA or [MTA]	My Talk Address	(via C)
OSA	Other Secondary Address	(via C)
OTA	Other Talk Address	(via C)
PCG	Primary Command Group	(via C)
PPC	Parallel Poll Configure	(via C)
[PPD]	Parallel Poll Disable	(via C)
[PPE]	Parallel Poll Enable	(via C)
PPR_N	Parallel Poll Response N	PP
PPU	Parallel Poll Unconfigure	(via C)
REN	Remote Enable	C
RFD	Ready for Data	AH
RQS	Request Service	T, TE
[SDC]	Selected Device Clear	(via C)
SPD	Serial Poll Disable	(via C)
SPE	Serial Poll Enable	(via C)
SRQ	Service Request	SR
STB	Status Byte	(via T, TE)
TCT	Take Control	(via C)
UNL	Unlisten	(via C)

**All Controller messages must be sent via Intel's 8292.

8291 Registers

A bit-by-bit map of the 16 registers on the 8291 is presented in Table 3. A more detailed explanation of each of these registers and their functions follows. The access of these registers by the microprocessor is accomplished by using the $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, and RS_0-RS_2 pins.

Register	$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	RS_0-RS_2
All Read Registers	0	0	1	CCC
All Write Registers	0	1	0	CCC
Don't Care	1	X	X	XXX

TABLE 3. 8291 REGISTERS

READ REGISTERS								REGISTER SELECT CODE			WRITE REGISTERS							
								RS2	RS1	RS0								
DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0	0	0	0	DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0
DATA IN											DATA OUT							
CPT	APT	GET	END	DEC	ERR	BO	BI	0	0	1	CPT	APT	GET	END	DEC	ERR	BO	BI
INTERRUPT STATUS 1											INTERRUPT MASK 1							
INT	SPAS	LLO	REM	SPASC	LLOC	REMC	ADSC	0	1	0	0	0	DMAO	DMAI	SPASC	LLOC	REMC	ADSC
INTERRUPT STATUS 2											INTERRUPT MASK 2							
S8	SRQS	S6	S5	S4	S3	S2	S1	0	1	1	S8	rsv	S6	S5	S4	S3	S2	S1
SERIAL POLL STATUS											SERIAL POLL MODE							
ton	lon	EOI	LPAS	TPAS	LA	TA	MJMN	1	0	0	TO	LO	0	0	0	0	ADM1	ADM0
ADDRESS STATUS											ADDRESS MODE							
CPT7	CPT6	CPT5	CPT4	CPT3	CPT2	CPT1	CPT0	1	0	1	CNT2	CNT1	CNT0	COM4	COM3	COM2	COM1	COM0
COMMAND PASS THROUGH											AUX MODE							
X	DT0	DL0	AD5-0	AD4-0	AD3-0	AD2-0	AD1-0	1	1	0	ARS	DT	DL	AD5	AD4	AD3	AD2	AD1
ADDRESS 0											ADDRESS 0/1							
X	DT1	DL1	AD5-1	AD4-1	AD3-1	AD2-1	AD1-1	1	1	1	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0
ADDRESS 1											EOS							

Data Registers

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0

DATA-IN REGISTER (0R)

DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0

DATA-OUT REGISTER (0W)

The data-in register is used to move data from the GPIB to the microprocessor or to memory when the 8291 is addressed to listen. Incoming information is separately latched by this register, and its contents are not destroyed by a write to the data-out register. The RFD (Ready for Data) message is held false until the byte is removed from the data in register, either by the microprocessor or by DMA. The 8291 then completes the handshake automatically. In RFD/DAV holdoff mode (see Auxiliary Register A), the handshake is not finished until a command is sent telling the 8291 to release the holdoff. In this way, the same byte may be read several times, or an over anxious talker may be held off until all available data has been processed.

When the 8291 is addressed to talk, it uses the data-out register to move data onto the GPIB. Upon a write to this register, the 8291 initiates and completes the handshake while sending the byte out over the bus. When the RFD/DAV holdoff mode is in effect, data is held until the release command is issued. Also, a read of the data-in register does not destroy the information in the data-out register.

Interrupt Registers

CPT	APT	GET	END	DEC	ERR	BO	BI

INTERRUPT STATUS 1 (1R)

CPT	APT	GET	END	DEC	ERR	BO	BI

INTERRUPT MASK 1 (1W)

INT	SPAS	LLO	REM	SPASC	LLOC	REMC	ADSC

INTERRUPT STATUS 2 (2R)

0	0	DMAO	DMAI	SPASC	LLOC	REMC	ADSC

INTERRUPT MASK 2 (2W)

The 8291 can be configured to generate an interrupt to the microprocessor upon the occurrence of any of 12 conditions or events on the GPIB. Upon receipt of an interrupt, the microprocessor must read the Interrupt Status registers to determine which event has occurred, and then execute the appropriate service routine (if necessary). Each of the 12 interrupt status bits has a matching mask bit in the interrupt mask registers. These mask bits are used to select the events that will cause the INT pin to be asserted. Writing a logic "1" into any of these bits enables the corresponding interrupt status bits to generate an interrupt. Bits in the Interrupt Status registers are set regardless of the states of the mask bits. The Interrupt Status registers are then cleared upon being read or when a local pon (power-on) message is executed. If an event occurs while one of the Interrupt Status registers is being read, the event is typically held until after its register is cleared and then placed in the register.

The mnemonics for each of the bits in these registers and a brief description of their respective functions appears in Table 4. This table also indicates how each of the interrupt bits is set.

TABLE 4. Interrupt Bits

Indicates Undefined Commands	CPT	An undefined command has been received.
Set by (TPAS + LPAS)•SCG•ACDS•MODE 3	APT	A secondary address must be passed through to the microprocessor for recognition.
Set by DTAS	GET	A group execute trigger has occurred.
Set by (EOS + EOI)•LACS	END	An EOS or EOI message has been received.
Set by DCAS	DEC	Device Clear Active State has occurred.
Set by TACS•nba•DAC•RFD	ERR	Interface error has occurred; no listeners are active.
TACS•(SWNS + SGNS)	BO	A byte has been output.
Set by LACS•ACDS	BI	A byte has been input.
Shows status of the INT pin	INT	These are status only. They will not generate interrupts, nor do they have corresponding mask bits.
The device has been enabled for a serial poll	SPAS	
The device is in local lock out state. (LWLS+RWLS)	LLO	
The device is in a remote state. (REMS+RWLS)	REM	
SPAS ⇄ $\overline{SPAS}$	SPASC	Serial Poll Active State change interrupt
LLO ⇄ NO LLO	LLOC	Local lock out change interrupt.
Remote ⇄ Local	RLC	Remote/Local change interrupt.
Addressed ⇄ Unaddressed	ADSC	Address status change interrupt.*

*In ton (talk-only) and lon (listen-only) modes, no ADSC interrupt is generated.

The BO and BI interrupts enable the user to perform data transfer cycles. BO indicates that a byte has been sent to the GPIB and a new data byte may be written into the Data Out register. It is set by the occurrence of TACS • (SWNS + SGNS). Hence, it is reset when a data byte is written into the Data Out register, when ATN is asserted on the GPIB, or when the device stops being addressed to talk. Similarly, BI is set when an input byte is accepted into the 8291 and reset when the microprocessor reads the Data In register. BO and BI are also reset by pon (power-on local message) and by a read of the Interrupt Status 1 register. However, if it is so desired, data transfer cycles may be performed without reading the Interrupt Status 1 register if all interrupts except for BO or BI are masked; BO and BI will automatically reset after each byte is transferred.

If the 8291 is used without DMA, the BO and BI interrupts may be enabled through the DMA REQ pin. The DMAO and DMAI bits in the Interrupt Mask 2 register would be the corresponding mask bits for this feature. Thus, implementing this feature, with BO and BI masked from the INT pin, allows for servicing of these interrupts without reading the Interrupt Status registers.

The ERR bit is set to indicate the bus error condition where the 8291 is an active talker, tries sending a byte to the GPIB, but there are no active listeners (e.g., all devices on the GPIB are in AIDS). The logical equivalent of (nba • TACS • DAC • RFD) will set this bit.

The DEC bit is set whenever DCAS has occurred. The user must define a known state to which all device functions will return in DCAS. Typically this state will be a power-on state. However, the state of the device functions at DCAS is at the designer's discretion. It should be noted that DCAS has no effect on the interface functions which are returned to a known state by the IFC (interface clear) message or the pon local message.

The End Interrupt bit may be used by the microprocessor to detect that a multi-byte transfer has been completed. The bit will be set when the 8291 is an active listener (LACS) and either EOS or EOI is received. EOS will generate an interrupt when the byte in the Data In register matches the byte in the EOS register. Otherwise the interrupt will be generated when a true input is detected at the EOI pin of the 8291.

The GET interrupt bit is used by the microprocessor to detect that DTAS has occurred. It is set by the 8291 when the GET message is received while it is addressed to listen. The TRIG output pin of the 8291 is also asserted when the GET message is received. Thus, the basic operation of the device may be started without involving the microprocessor.

The APT interrupt bit indicates to the processor that a secondary address is available in the CPT register for validation. This interrupt will only occur if Mode 3 addressing is in effect. (Refer to the section on addressing.) In Mode 2, secondary addresses will be recognized on the 8291. They will be ignored in Mode 1.

The CPT interrupt bit flags the occurrence of an undefined command and of all secondary commands following an undefined command. The Command pass through feature is enabled by the BO bit of Auxiliary register B.

$$UDC = [UCG + ACG(TADS \bullet \overline{PPC} + LADS \bullet \overline{TCT})] \bullet undefined \bullet BO$$

where:

ACG — Addressed Command Group
UCG — Universal Command Group
SCG — Secondary Command Group

Any message not decoded by the 8291 (not included in the state diagrams in Appendix B) becomes an undefined command. Note from the logic equation that any addressed command is automatically ignored when the 8291 is not addressed.

Undefined commands are read by the CPU from the Command Pass Through Register of the 8291. Until this register is read, the 8291 will hold off the handshake (only if the CPT feature is enabled).

An especially useful feature of the 8291 is its ability to generate interrupts from state transitions in the interface functions. In particular, the lower 4 bits of the Interrupt Status 2 register, if enabled by the corresponding mask bits, will cause an interrupt upon changes in the following states as defined in IEEE 488:

Bit 0	ADSC	change in LIDS or TIDS or MJMN
Bit 1	RLC	change in LOCS or REMS
Bit 2	LLOC	change in LWLS or RWLS
Bit 3	SPASC	change in SPAS

The upper 4 bits of the Interrupt Status 2 register are available to the processor as status bits. Thus, if one of the bits 1-3 generates an interrupt indicating a state change has taken place, the corresponding status bit (bits 5-7) may be read to determine what the new state is. To determine the nature of a change in addressed status (bit 0) the Address Status Register is available to be read. And finally, bit 7 monitors the state of the 8291 INT pin. Logically, it is an OR of all unmasked interrupt status bits. One should note that bits 4-7 of the Interrupt Status 2 Register do not generate interrupts, but are available only to be read as status bits by the processor.

Bits 4 and 5 (DMAI, DMAO) of the Interrupt Mask 2 Register are available to enable direct data transfers between memory and the GPIB, DMAI (DMA in) enables the DMA REQ (DMA request) pin of the 8291 to be asserted upon the occurrence of BI. Similarly, DMAO (DMA out) enables the DMA REQ pin to be asserted upon the occurrence of BO. One might note that the DMA REQ pin may be used as a second interrupt output pin, monitoring BI and/or BO and masked by DMAI and DMAO. One should note that the DMA REQ pin is not affected by a read of the Interrupt Status 1 Register. It is reset whenever a byte is written to the Data Out Register or read from the Data in Register.

To ensure that an interrupt status bit will not be cleared without being read, and will not remain uncleared after being read, the 8291 implements a special interrupt

handling procedures. When an unmasked interrupt bit is set in either of the Interrupt Status Registers, the input of the registers are blocked until the set bit is read and reset by the microprocessor. Thus, potential problems arise when interrupt status changes while the register is being blocked. However, the 8291 stores all new interrupts in a temporary register and transfers them to the appropriate interrupt Status Register after the interrupt has been reset. In the Interrupt Status 1 Register and in ADSC bit, this transfer takes place only if the corresponding bits were read as zeroes. For the other status change bits in the Interrupt Status 2 Register, the transfer will always take place. However, even number of changes in these status bits during blocking time will cause no interrupt.

Serial Poll Registers

S8	SRQS	S6	S5	S4	S3	S2	S1

SERIAL POLL STATUS (3R)

S8	rsv	S6	S5	S4	S3	S2	S1

SERIAL POLL MODE (3W)

The Serial Poll Mode Register is used to establish the status byte that the 8291 sends out on the GPIB data lines when it receives the SPE (Serial Poll Enable) message. Bit 6 of this register is reserved for the rsv (request service) local message. Setting this bit to 1 causes the 8291 to assert its SRQ line, indicating its need for attention from the controller-in-charge of the GPIB. When service has been granted, the bit should be cleared by the microprocessor. The other bits of this register are available for sending status information over the GPIB. Sometime after the microprocessor initiates a request for service by setting bit 6, the controller of the GPIB sends the SPE message and then addresses the 8291 to talk. At this point, one byte of status is returned by the 8291 via the Serial Poll Mode Register.

The Serial Poll Status Register is available for reading the status byte in the Serial Poll Mode Register. The processor may check the status of a request for service by polling bit 6 of this register, which corresponds to SRQS (Service Request State). When a Serial Poll is conducted and the controller-in-charge reads the status byte, the SRQS bit is cleared. The SRQ line is tied to this bit, so that a request for service is terminated when the 8291's status byte is read. The rsv bit of the Serial Poll Mode Register must then be cleared by the microprocessor.

Address Registers

ton	lon	EOI	LPAS	TPAS	LA	TA	MJMN

ADDRESS STATUS (4R)

TO	LO	0	0	0	0	ADM1	ADM0

ADDRESS MODE (4W)

X	DT0	DL0	AD5-0	AD4-0	AD3-0	AD2-0	AD1-0

ADDRESS 0 (6R)

ARS	DT	DL	AD5	AD4	AD3	AD2	AD1

ADDRESS 0/1 (6W)

X	DT1	DL1	AD5-1	AD4-1	AD3-1	AD2-1	AD1-1

ADDRESS 1 (7R)

The Address Mode Register is used to select one of the five modes of addressing available on the 8291. It determines the way in which the 8291 uses the information in the Address 0 and Address 1 registers:

—In Mode 1, the contents of the Address 0 Register constitute the "Major" talker/listener address while the Address 1 Register represents the "Minor" talker/listener address. In applications where only one address is needed, the major talker/listener is used, and the minor talker/listener should be disabled. Loading an addres via the Address 0/1 Register into Address Registers 0 and 1 enables the major and minor talker/listener functions respectively.

—In Mode 2 the 8291 recognizes two sequential address bytes: a primary followed by a secondary. Both address bytes must be received in order to enable the device to talk or listen. In this manner, Mode 2 addressing implements the extended talker and listener functions as defined in IEEE 488.

To use Mode 2 addressing the primary address must be loaded into the Address 0 Register, and the Secondary address is placed in the Address 1 Register. With both primary and secondary addresses residing on chip, the 8291 can handle all addressing sequences without processor intervention.

—In Mode 3, the 8291 handles addressing just as it does in Mode 1, except that each Major or Minor primary address must be followed by a secondary address. All secondary addresses must be verified by the microprocessor when Mode 3 is used. When the 8291 is in TPAS or LPAS (talker/listener primary addresses state), and it does not recognize the byte on the DIO lines, an APT interrupt is generated (see section on Interrupt Registers) and the byte is available in the CPT (Command Pass-Through) Register. As part of its interrupt service routine, the microprocessor must read the CPT Register and write one of the following responses to the Auxiliary Mode Register:

1. 07H implies a non-valid secondary address
2. 0FH implies a valid secondary address

Setting the "ton" bit generates the local ton (talk-only) message and sets the 8291 to a talk-only mode. This mode allows the device to operate as a talker in an interface system without a controller.

Setting the "lon" bit generates the local lon (listen-only) message and sets the 8291 to a listen-only mode. This mode allows the device to operate as a listener in an interface system without a controller.

The mode of addressing implemented by the 8291 may be selected by writing one of the following bytes to the Address Mode Register:

Register Contents	Mode
10000000	Enable talk only mode (ton)
01000000	Enable listen only mode (lon)
11000000	The 8291 may talk to itself
00000001	Mode 1, (Primary-Primary)
00000010	Mode 2 (Primary-Secondary)
00000011	Mode 3 (Primary/APT-Primary/APT)

The Address Status Register contains information used by the microprocessor to handle its own addressing. This information includes status bits that monitor the address state of each talker/listener, "ton" and "lon" flags which indicate the talk only and listen only states, and an EOI bit which, when set, signifies that the END message came with the last data byte. LPAS and TPAS indicate that the listener or talker primary address has been received. The microprocessor can then use these bits when the secondary address is passed through to determine whether the 8291 is addressed to talk or listen. The LA (listener addressed) bit will be set when the 8291 is in LACS (Listener Active State) or in LADS (Listener Addressed State). Similarly, the TA (Talker Addressed bit will be set to indicate TACS or TADS, but also to indicate SPAS (Serial Poll Active State). The MJMN bit is used to determine whether the information in the other bits applies to the Major or Minor talker/listener. It is set to "1" when the Minor talker/listener is addressed. It should be noted that only one talker/listener may be active at any one time. Thus, the MJMN bit will indicate which, if either, of the talker/listeners is addressed or active.

The Address 0/1 Register is used for specifying the device's addresses according to the format selected in the Address Mode Register. Five bit addresses may be loaded into the Address 0 and Address 1 registers by writing into the Address 0/1 Register. The ARS bit is used to select which of these registers the other seven bits will be loaded into. The DT and DL bits may be used to disable the talker or listener function at the address signified by the other five bits. When Mode 1 addressing is used and only one primary address is desired, both the talker and the listener should be disabled at the Minor address.

As an example of how the Address 0/1 Register might be used, consider an example where two primary addresses are needed in the device. The Major primary address will be selectable only as a talker and the Minor primary address will be selectable only as a listener. This configuration of the 8291 is formed by the following sequence of writes by the microprocessor:

Operation	$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	Data	RS2-RS0
1. Select addressing Mode 1	0	1	0	00000001	100
2. Load major address into Address 0 Register with listener function disabled.	0	1	0	001AAAAA	110
3. Load minor address into Address 1 Register with talker function disabled.	0	1	0	110BBBBB	110

At this point, the addresses AAAAA and BBBBB are stored in the Address 0 and Address 1 registers respectively, and are available to be read by the microprocessor. Thus, it is not necessary to store any address information elsewhere. Also, with the information stored in the Address 0 and Address 1 registers, processor intervention is not required to recognize addressing by the controller. Only in Mode 3, where secondary addresses are passed through, must the processor intervene in the addressing sequence.

Command Pass Through Register

CPT7	CPT6	CPT5	CPT4	CPT3	CPT2	CPT1	CPT0

COMMAND PASS THROUGH (5R)

The Command Pass Through Register is used to transfer undefined 8-bit remote message codes from the GPIB to the microprocessor. When the CPT feature is enabled (bit B0 in Auxiliary Register B), any message not decoded by the 8291 becomes an undefined command. When Mode 3 addressing is used secondary addresses are also passed through the CPT Register. In either case, the 8291 will holdoff the handshake until the microprocessor reads this register and issues the VSCMD auxiliary command.

The CPT and APT interrupts flag the availability of undefined commands and secondary addresses in the CPT Register. The details of these interrupts are explained in the section on Interrupt Registers.

An added feature of the 8291 is its ability to handle undefined secondary commands following undefined primaries. Thus, the number of available commands for user definition or future IEEE 488 definition is significantly increased; one undefined primary command followed by a sequence of as many as 32 secondary commands can be processed. However, it is recommended that users do not define their own commands since such definition would violate IEEE 488.

The recommended use of the 8291's undefined command capabilities is for a controller-configured Parallel Poll. The PPC message is an undefined primary command typically followed by PPE, an undefined secondary command. For details on this procedure, refer to the section on Parallel Poll Protocol.

Auxiliary Mode Register

CNT2	CNT1	CNT0	COM4	COM3	COM2	COM1	COM0

AUX MODE (5W)

CNT0—2:CONTROL BITS
COM0—:COMMAND BITS

The Auxiliary Mode Register contains a three-bit control field and a five-bit command field. It is used for several purposes on the 8291:

1. To load "hidden" auxiliary registers on the 8291.
2. To issue commands from the microprocessor to the 8291.
3. To preset an internal counter used to generate T1, delay in the Source Handshake function, as defined in IEEE 488.

Table 4 summarizes how these tasks are performed with the Auxiliary Mode Register. Note that the three control bits determine how the five command bits are interpreted.

TABLE 4

CODE		COMMAND
CONTROL BITS	COMMAND BITS	
000	0CCCC	Execute auxiliary command CCCC
001	0FFFF	Preset internal counter to match external clock frequency of FFFF MHZ (FFFF - binary representation of 1 to 8 MHz)
100	DDDDD	Write DDDDD into auxiliary register A
101	0DDDD	Write DDDD into auxiliary register B
011	$USP_3P_2P_1$	Configure/unconfigure parallel poll $SP_3P_2P_1$ as defined in Std. 488. (Configure if U = 0, Unconfigure if U = 1). This command is the local poll enable (lpe) message when U = 0.

AUXILIARY COMMANDS

Auxiliary commands are executed by the 8291 whenever 0000CCCC is written into the Auxiliary Mode Register, where CCCC is the 4-bit command code.

4-Bit Code	Description
0000	Immediate Execute pon — This command resets the 8291 to a power up state (local pon message as defined in IEEE 488). The following conditions constitute the power up state: 1. All talkers and listeners are disabled. 2. No interrupt status bits are set. The 8291 is designed to power up in certain states as specified in the IEEE 488 state diagrams. Thus, the following states are in effect in the power up state: SIDS, AIDS, TIDS, LIDS, NPRS, LOCS, and PPIS. The "0000" pon is an immediate execute command (a pon pulse). It is also used to release the "initialize" state generated by either an external reset pulse or the "0010" Chip Reset command.
0010	Chip Reset (Initialize) — This command has the same effect as a pulse applied to the Reset pin. (Refer to the section on Reset Procedure.)
0011	Finish Handshake — This command finishes a handshake that was stopped because of a holdoff on RFD or DAV. (Refer to Auxiliary Register A.)
0100	Trigger — A "Group Execute Trigger" is forced by this command. It has the same effect as a GET command issued by the controller-in-charge of the GPIB, but does not cause a GET interrupt.
0101	rtl[1] — This command corresponds to the local rtl message as defined in IEEE 488. The 8291 will go to a local state if local lockout is not in effect.
0110	Send EOI — The EOI line of the 8291 may be asserted with this command. The command causes EOI to go true with the next byte transmitted. The EOI line is then cleared upon completion of the handshake for that byte.
0111, 1111	Non-Valid/Valid Secondary Address or Command (VSCMD) — This command informs the 8291 that the secondary address received by the microprocessor was valid or invalid (0111 → invalid, 1111 → valid). If Mode 3 addressing is used, the processor must field each extended address and respond to it, or the GPIB will hang up. Note that the COM3 bit is the invalid/valid flag. The valid (1111) command is also used to tell the 8291 to continue from the command-pass-through state (immediate execute command).
0001, 1001	Parallel Poll Flag (local "ist" message) — This command sets (1001) or clears (0001) the parallel poll flag. A "1" is sent over the assigned data line (PPR-Parallel Poll Response true) only if the parallel poll flag matches the sense bit from the lpe local message (or indirectly from the PPE message). For a more complete description of the Parallel Poll features and procedures refer to the section on Parallel Poll Protocol.

1. Subsequently the 8291 will include "set rtl" and "clear rtl" commands.

INTERNAL COUNTER

The internal counter determines the delay time allowed for the settling of data on the DIO lines. This delay time is defined as T_1 in IEEE 488 and appears in the Source Handshake state diagram between SDYS and STRS. As such, DAV is asserted T_1 *after* the DIO lines are driven. Consequently, T_1 is a major factor in determining the data transfer rate of the 8291 over the GPIB (T_1 = TWROV2-TWROI5).

When open-collector transceivers are used for connection to the GPIB, T_1 is defined by IEEE 488 to be 2μsec. By writing 0010FFFF into the Auxiliary Mode Register, the counter is preset to match a f_C MHz clock input, where FFFF is the binary representation of N_F ($1 \leq N_F \leq 8$, $N_F = (FFFF)_2$). When $N_F = f_C$, a 2μsec T_1 delay will be generated before each DAV asserted.

$$T_{1(\mu sec)} = \frac{2N_F}{f_C} + t_{SYNC}\ ,\ 1 \leqslant N_F \leqslant 8$$

t_{SYNC} is a synchronization error, greater than zero and smaller than the larger of T clock high and T clock low. (For a 50% duty cycle clock, t_{SYNC} is less than half the clock cycle).

If it is necessary that T_1 be different from 2μsec, N_F may be set to a value other than f_C. In this manner, data transfer rates may be programmed for a given system. In small systems, for example, where transfer rates exceeding GPIB specifications are required, one may set $N_F < f_C$ and decrease T_1.

When tri-state transceivers are used, IEEE 488 allows a higher transfer rate (lower T_1). Use of the 8291 with such transceivers is enabled by setting B2 in Auxiliary Register B.In this case, setting $N_F = f_C$ causes a T_1 delay of 2μsec to be generated for the first byte transmitted — all subsequent bytes will have a delay of 500 nsec.

$$T_1(\text{High Speed})\ \mu sec = \frac{N_F}{2f_C} + t_{SYNC}$$

Thus, setting $N_F = 1$ using a 4 MHz clock will generate for a 50% duty cycle clock (t_{SYNC}<125 nsec.):

$$T_1 = \frac{1}{2.4} + 0.125 = 0.250\ \mu sec = 250\ nsec$$

AUXILIARY REGISTER A

Auxiliary Register A is a "hidden" 5-bit register which is used to enable some of the 8291 features. Whenever a 100 $A_4A_3A_2A_1A_0$ byte is written into the Auxiliary Register, it is loaded with the data $A_4A_3A_2A_1A_0$. Setting the respective bits to "1" enables the following features:

A_0 — RFD/DAV Holdoff on all Data: If the 8291 is listening, RFD will not be sent true until the "finish handshake" auxiliary command is issued by the microprocessor. If the 8291 is talking, DAV is not sent true until the "finish handshake" command is given. In both cases, the holdoff will be in effect for each data byte.

A_1 — RFD/DAV Holdoff on End: This feature enables the holdoff on EOI or EOS (if enabled). However, no holdoff will be in effect on any other data bytes.

A_2 — End on EOS Received: Whenever the byte in the Data In Register matches the byte in the EOS Register, the End interrupt bit will be set in the Interrupt Status 1 Register.

A_3 — Output EOI on EOS Sent: Any occurrence of data in the Data Out Register matching the EOS Register causes the EOI line to be sent true along with the data.

A_4 — EOS Binary Compare: Setting this bit causes the EOS Register to function as a full 8-bit word. When it is not set, the EOS Register is a 7-bit word (for ASCII characters).

If $A_0 = A_1 = 1$, a special "continuous Acceptor Handshake cycling" mode is enabled. This mode should be used only in a controller system configuration, where both the 8291 and the 8292 are used. It provides a continuous cycling through the Acceptor Handshake state diagram, requiring no local messages from the microprocessor; the rdy local message is automatically generated when in ANRS. As such, the 8291 Acceptor Handshake serves as the controller Acceptor Handshake. Thus, the controller cycles through the Acceptor Handshake without delaying the data transfer in progress. When the t_{CS} local message is executed, the 8291 is taken out of the "continuous AH cycling" mode, the GPIB hangs up in ANRS, and a BI interrupt is generated to indicate that control may be taken. A simpler procedure may be used when a "t_{CS} on end of block" is executed; the 8291 may stay in "continuous AH cycling". Upon the end of a block (EOI or EOS received), a holdoff is generated, the GPIB hangs up in ANRS, and control may be taken.

AUXILIARY REGISTER B

Auxiliary Register B is a "hidden" 4-bit register which is used to enable some of the features of the 8291. Whenever a 1010$B_3B_2B_1B_0$ is written into the Auxiliary Mode Register, it is loaded with the data $B_3B_2B_1B_0$. Setting the respective bits to "1" enables the following features:

B_0 — Enable Undefined Command Pass Through: This feature allows any commands not recognized by the 8291 to be handled in software. If enabled, this feature will cause the 8291 to holdoff the handshake when an undefined command is received. The microprocessor must then read the command from the Command Pass Through Register and send the VSCMD auxiliary command. Until the VSCMD command is sent, the handshake holdoff will be in effect.

B_1 — Send EOI in SPAS: This bit enables EOI to be sent with the status byte; EOI is sent true in Serial Poll Active State. Otherwise, EOI is sent false in SPAS.

B_2 — Enable High Speed Data Transfer: This feature may be enabled when tri-state external transceivers are used. The data transfer rate is limited by T_1 (delay time generated in the Source Handshake function), which is defined according to the type of transceivers used. When the "High Speed" feature is enabled, T_1 = 2 microseconds is generated for the first byte transmitted after each true to false transition of ATN. For all subsequent bytes, T_1 = 500 nanoseconds. Refer to the Internal Counter section for an explanation of T_1 duration as a function of B_2 and of clock frequency.

B_3 — Enable Active Low Interrupt: Setting this bit causes the polarity of the INT pin to be reversed, providing an output signal compatible with Intel's MCS-48™. Interrupt registers are not affected by this bit.

PARALLEL POLL PROTOCOL

Writing a 011USP$_3$P$_2$P$_1$ into the Auxiliary Mode Register will configure (U=0) or unconfigure (U=1) the 8291 for a parallel poll. When U=0, this command is the "lpe" (local poll enable) local message as defined in IEEE 488. The "S" bit is the sense in which the 8291 is configured; only if the Parallel Poll Flag ("ist" local message) matches this bit will the Parallel Poll Response, PPR$_N$, be sent true. The bits P$_3$P$_2$P$_1$ specify which of the eight data lines PPR$_N$ will be sent over. Thus, once the 8291 has been configured for Parallel Poll, whenever it senses both EOI and ATN true, it will automatically compare its PP flag with the sense bit and send PPR$_N$ true or false according to the comparison.

If a PP$_2$* implementation is desired, the "lpe" and "ist" local messages are all that are needed. Typically, the user will configure the 8291 for Parallel Poll immediately after initialization. During normal operation the microprocessor will set or clear the Parallel Poll Flag (ist) according to the device's need for service. Consequently the 8291 will be set up to give the proper response to IDY (EOI • ATN) without directly involving the microprocessor.

If a PP1* implementation is desired, the undefined command features of the 8291 must be used. In PP1, the 8291 is indirectly configured for Parallel Poll by the active controller on the GPIB. The sequence at the 8291 being configured is as follows:

1. The PPC message is received true. Being an undefined command, it is loaded into the Command Pass Through Register, and a CPT interrupt is sent to the microprocessor. The handshake is automatically held off.

2. The microprocessor reads the CPT Register and sends VSCMD to the 8291, releasing the handshake.

3. Having received an undefined primary command, the 8291 is set up to receive an undefined secondary command, the PPE message. This message is also received into the CPT Register, the handshake is held off, and the CPT interrupt is generated.

4. The microprocessor reads the PPE message and decodes the SP$_3$P$_2$P$_1$ information. It then sends the appropriate "lpe" local message to the 8291. Finally, the microprocessor sends VSCMD and the handshake is released.

*As defined in IEEE Standard 488.

End of Sequence (EOS) Register

EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0

EOS REGISTER

The EOS Register and its features offer an alternative to the "Send EOI" auxiliary command. A seven or eight bit byte (ASCII or binary) may be placed in the register to flag the end of a block or read. The type of EOS byte to be used is selected in Auxiliary Register bit A$_4$.

If the 8291 is a listener, and the "End on EOS Received" is enabled at bit A$_2$, then an End interrupt is generated in the Interrupt Status 1 Register whenever the byte in the Data-In Register matches the byte in the EOS Register.

If the 8291 is a talker, and the "Output EOI on EOS Sent" is enabled at bit A$_3$, then the EOI line is sent true with the next data byte whenever the contents of the Data Out Register match the EOS register.

Reset Procedure

The 8291 is reset to an initialization state either by a pulse applied to its Reset pin, or by a reset auxiliary command (02H written into the Auxiliary Command Register). The following conditions are caused by a reset pulse (or local reset command):

1. A "pon" local message as defined by IEEE 488 is held true until the initialization state is released.
2. The Interrupt Status Registers are cleared.
3. Auxiliary Registers A and B are cleared.
4. The Serial Poll Mode Register is cleared.
5. The Parallel Poll Flag is cleared.
6. The EOI bit in the Address Status Register is cleared.
7. N_F in the Internal Counter is set to 8 MHz. This setting causes the longest possible t_1 delay to be generated in the Source Handshake (16 μsec for 1 MHz clock).

The initiallization state is released by an "immediate execute pon" command (00H written into the Auxiliary Command Register).

The suggested initialization sequence is:

1. Apply a reset pulse or send the reset auxiliary command.
2. Set the desired initial conditions by writing into the Interrupt Mask, Serial Poll Mode, Address Mode, Address 0/1, and EOS Registers. Auxiliary Registers A and B, and the internal counter should also be initialized.
3. Send the "immediate execute pon" auxiliary command to release the initialization state.
4. If a PP$_2$ Parallel Poll implementation is to be used the "lpe" local message may be sent, configuring the 8291 for a Parallel Poll Response on an assigned line. (Refer to the section on Parallel Poll Protocol.)

Using DMA

The 8291 may be connected to the Intel 8257 DMA Controller for DMA operation. The DMA REQ pin of the 8291 requests a DMA byte transfer from the 8257. It is set by BO or BI flip flops, masked by the DMAO and DMAI bits in the Interrupt Mask 2 Register. (After reading, the INT1 register BO and BI interrupts will be cleared but not BO and BI in DREQ equation.)

The $\overline{\text{DMA ACK}}$ pin is driven by the 8257 in response to the DMA request. When $\overline{\text{DMA ACK}}$ is true (active low) it sets CS = RS0 = RS1 = RS2 = 0 such that the RD and WR signals sent by the 8257 refer to the Data In and Data Out Registers. Also, the DMA request line is reset by $\overline{\text{DMA ACK}}$.

DMA input sequence:

1. A data byte is accepted from the GPIB by the 8291.
2. A BI interrupt is generated and DMA REQ is set.
3. $\overline{\text{DMA ACK}}$ is asserted by the 8257 and DMA REQ is reset.
4. $\overline{\text{RD}}$ is driven by the 8257 and the contents of the Data In Register are transferred to MCS bus.
5. The 8291 sends RFD true on the GPIB and proceeds with the Acceptor Handshake protocol.

DMA output sequence:

1. A BO interrupt is generated (indicating that the Data Out Register is empty) and DMA REQ is asserted.
2. $\overline{\text{DMA ACK}}$ is asserted by the 8257 and DMA REQ is reset.
3. $\overline{\text{WR}}$ is driven by the 8257 and a byte is transferred from the MCS bus into the Data Out Register.
4. The 8291 sends DAV true on the GPIB and proceeds with the Source Handshake protocol.

It should be noted that each time the device is addressed, the Address Status Register should be read, and the 8257 should be initialized accordingly. (Refer to the 8257 data sheet available in Intel's Peripheral Design Handbook.)

System Configuration

Microprocessor Bus Connection

The 8291 is 8080, 8048, 8085 and 8086 compatible. The three address pins (RS_0, RS_1, RS_2) should be connected to the non-multiplexed address bus (for example: A_8, A_9, A_{10}). In case of 8080, any address lines may be used.

External Transceivers Connection

8291 IEEE bus pins are TTL compatible. For IEEE Std. bus connection, external transceivers are required. 8291 supplies Transmit/Receive control pins: T/R1 controls DIO_{1-8}, NRFD, NADC and DAV transceivers, T/R2 controls EOI transceiver. IFC, ATN, REN are always inputs and SRQ is always an output.

Logically, TR1 = TACS + SPAS + PPAS;
TR2 = TACS + SPAS.

Refer to 8292 Data Sheet for 8291/8292 system configuration.

DEVICE ELECTRICAL CHARACTERISTICS

D.C. CHARACTERISTICS

T_A = 0°C to 70°C; V_{CC} = 5V ± 10%

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL}=2mA (4mA for TR1 pin)
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400μA (-150μA for SRQ pin)
V_{OH-INT}	Interrupt Output High Voltage	2.4		V	I_{OH}=-400μA
		3.5		V	I_{OH}=-50μA
I_{IL}	Input Leakage		10	μA	V_{IN}=0V to V_{CC}
I_{LOL}	Output Leakage Current		-10	μA	V_{OUT}=0.45V
I_{LOH}	Output Leakage Current		10	μA	V_{OUT}=V_{CC}
I_{CC}	V_{CC} Supply Current		180	mA	T_A=0°C

A.C. CHARACTERISTICS

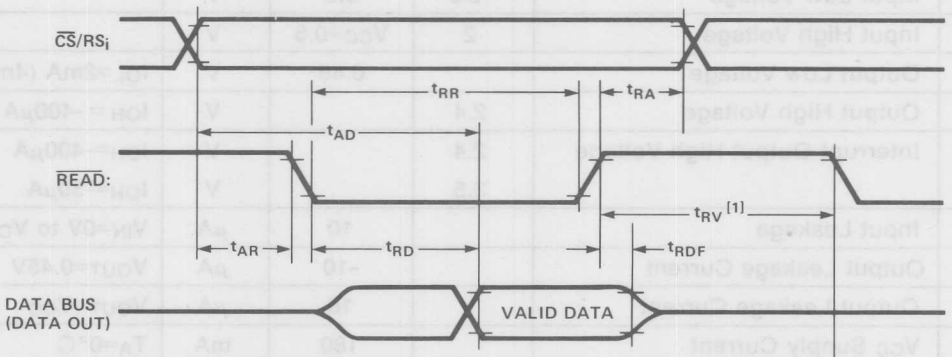
V_{CC} = 5V ± 10%, Commercial: T_A = 0°C to 70°C

Symbol	Parameter	Min.	Max.	Unit
t_{AR}	Address Stable Before $\overline{READ}$	0		nsec[1]
t_{RA}	Address Hold After $\overline{READ}$	0		nsec[1]
t_{RR}	$\overline{READ}$ width	250		nsec[2]
t_{AD}	Address Stable to Data Valid		250	nsec[1]
t_{RD}	$\overline{READ}$ to Data Valid		100	nsec[2]
t_{RDF}	Data Float After $\overline{READ}$	0	60[2]	nsec
t_{AW}	Address Stable Before $\overline{WRITE}$	0		nsec[1]
t_{WA}	Address Hold After $\overline{WRITE}$	0		
t_{WW}	$\overline{WRITE}$ Width	250		nsec[1]
t_{DW}	Data Set Up Time to the Trailing Edge of $\overline{WRITE}$	150		nsec[1]
t_{WD}	Data Hold Time After $\overline{WRITE}$	0		nsec[1]
t_{AKRQ}	$\overline{DACK}$↓ to DREQ↓		130	nsec
t_{DKDA6}	$\overline{DACK}$↓ to Up Data Valid		200	nsec

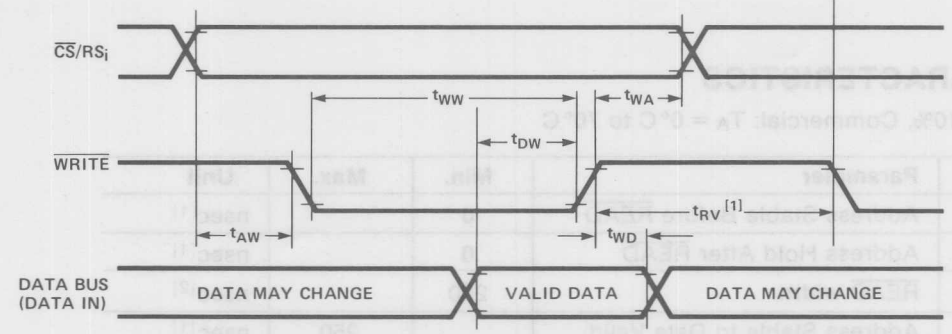
Notes:
1. 8080 System C_{Lmax} = 100pF; C_{Lmin} = 15pF; 3 MHz clock.
2. 8085 System C_L = 150pF; 4 MHz clock.

TIMING WAVEFORMS

READ

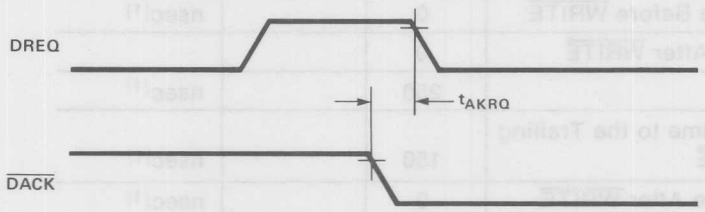


WRITE



NOTES: 1. t_{RV} IS THE TIME BETWEEN READ OR WRITE OPERATIONS WITH THE CHIP SELECTED (CHIP RECOVERY TIME).

DMA



GPIB TIMINGS[1]

Symbol	Parameter	Max.	Unit	Test Conditions
TEOT13	$\overline{EOI}$↓ to TR1↑	90	nsec	PPSS, $\overline{ATN}$=0.45V
TEODI6	$\overline{EOI}$↓ to $\overline{DIO}$ Valid	130	nsec	PPSS, $\overline{ATN}$=0.45V
TEOT12	$\overline{EOI}$↓ to TR1↓	130	nsec	PPSS, $\overline{ATN}$=0.45V
TATND4	$\overline{ATN}$↓ to $\overline{NDAC}$↓	130	nsec	TACS, AIDS
TATT14	$\overline{ATN}$↓ to TR1↓	130	nsec	TACS, AIDS
TATT24	$\overline{ATN}$↓ to TR2↓	130	nsec	TACS, AIDS
TDNVD3-C	$\overline{DAV}$↓ to $\overline{NDAC}$↑	350	nsec	AH, CACS
TNDDV1	$\overline{NDAC}$↑ to $\overline{DAV}$↑	300	nsec	SH, STRS
TNRDV2	$\overline{NRFD}$↑ to $\overline{DAV}$↓	300	nsec	SH, T1 True
TNDDR1	$\overline{NDAC}$↑ to DREQ↑	350	nsec	SH
TDVDR3	$\overline{DAV}$↓ to DREQ↑	350	nsec	AH, LACS, $\overline{ATN}$=2.4V
TDVND2-C	$\overline{DAV}$↑ to $\overline{NDAC}$↓	350	nsec	AH,LACS
TDVNR1-C	$\overline{DAV}$↑ to $\overline{NRFD}$↑	350	nsec	AH, LACS, rdy=True
TRDNR3	$\overline{RD}$↓ to $\overline{NRFD}$↑	500	nsec	AH, LACS
TWRDI5	$\overline{WR}$ to $\overline{DIO}$ Valid	200	nsec	SH, TACS, RS = 0.4V
TWRDV2	$\overline{WR}$↑ to $\overline{DAV}$↓	760	nsec	$\overline{NRFD}$ = 2.4V, RS = 0.4V, SH, TACS, High Speed Transfers Enabled, $N_F = f_C = 8$ MHz

Notes:
1. All GPIB timings are at the pins of the 8291.

Appendix A

MODIFIED STATE DIAGRAMS

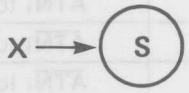
Figure A.1 presents the interface function state diagrams. It is derived from IEEE Std. state diagrams, with the following changes:

A. Controller function omitted.
B. Addressing modes included in T,L state diagrams.

Note that in Mode 3, MSA, OSA are generated only after secondary address validity check by the microprocessor (APT interrupt).

C. All remote messages sent true in each state are indicated.
D. All remote multiline messages decoded are conditioned by ACDS. The multiplication by ACDS is not drawn to simplify the diagrams.

E. The symbol



indicates:

1. When event X occurs, the function will return to state S.
2. X overrides any other transition condition in the function.

Statement 2 simplifies the diagram, avoiding the explicit use of $\overline{X}$ to condition all transitions from S to other states.

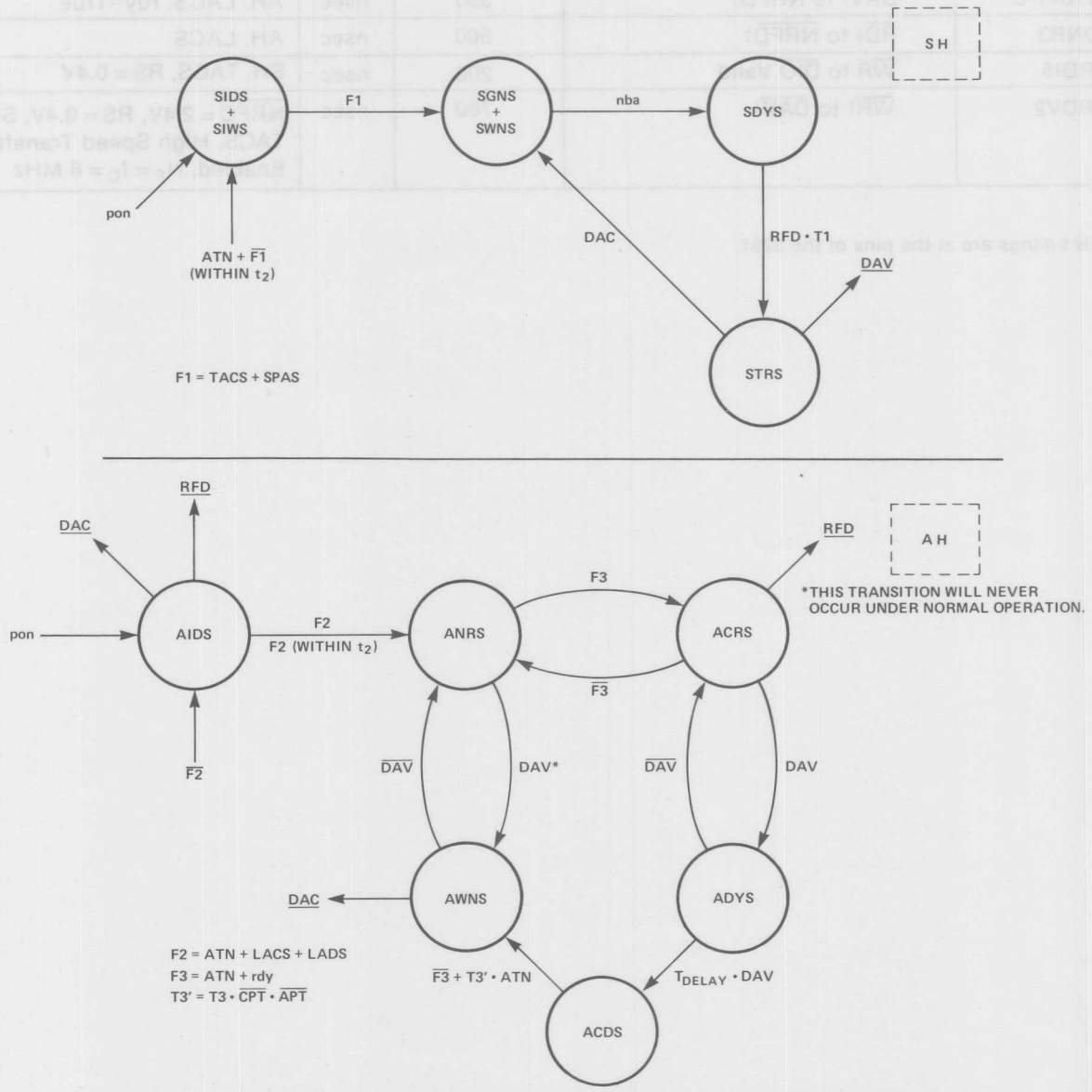


Figure A.1. 8291 State Diagrams (Continued next page)

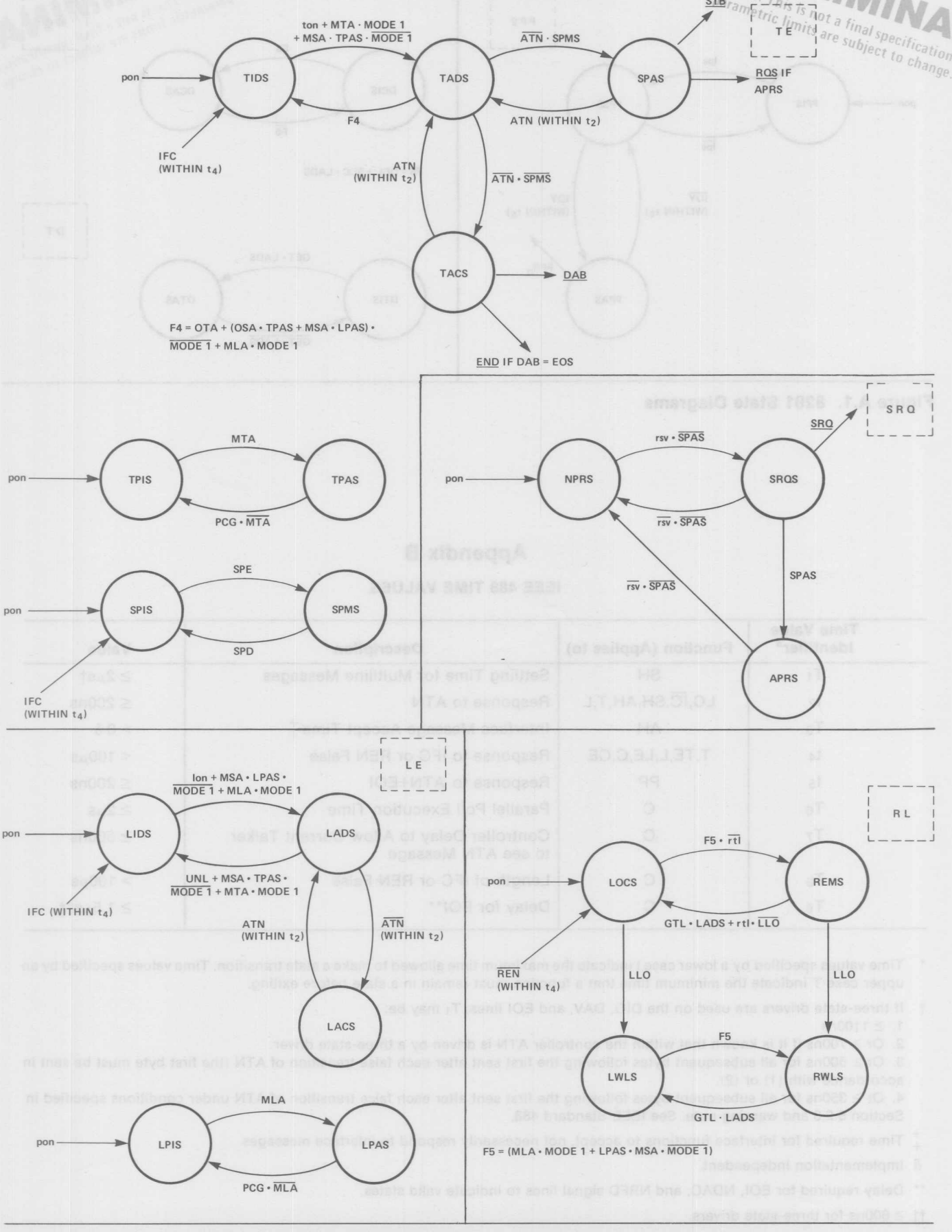


Figure A.1. 8291 State Diagrams (Continued next page)

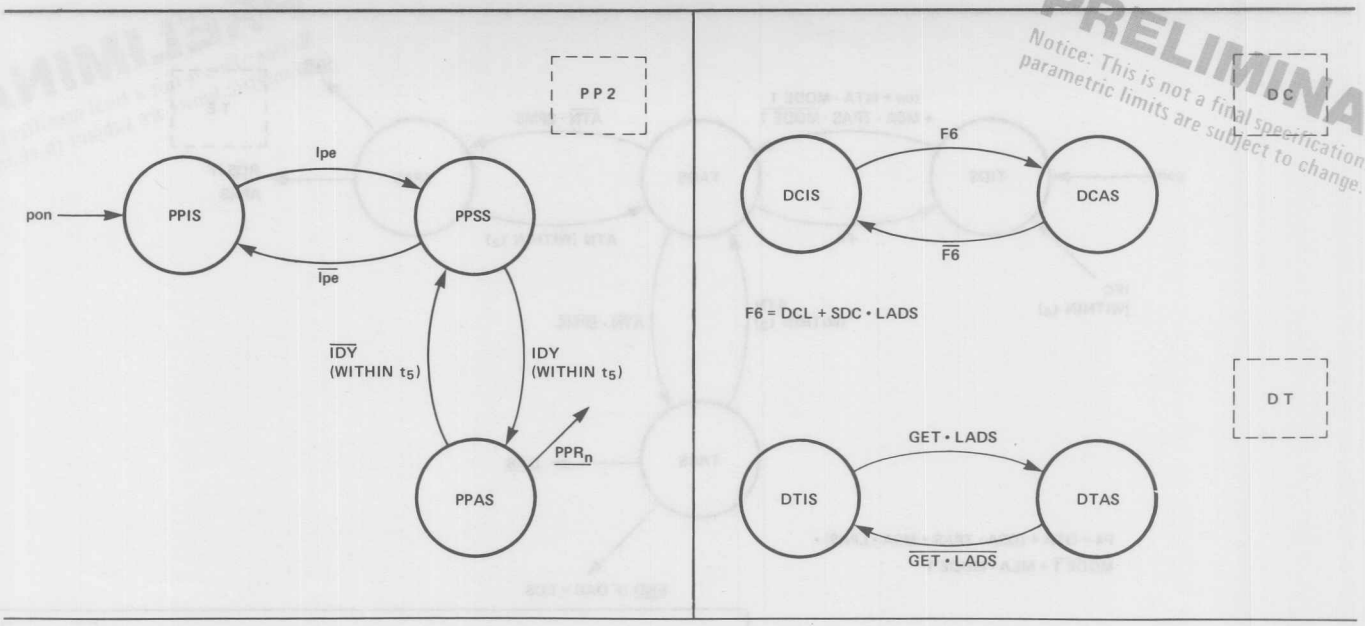


Figure A.1. 8291 State Diagrams

Appendix B

IEEE 488 TIME VALUES

Time Value Identifier*	Function (Applies to)	Description	Value
T_1	SH	Settling Time for Multiline Messages	$\geq 2\mu s$†
t_2	LC,$\overline{IC}$,SH,AH,T,L	Response to ATN	$\leq$ 200ns
T_3	AH	Interface Message Accept Time ‡	$> 0\,\delta$
t_4	T,TE,L,LE,C,CE	Response to IFC or REN False	$< 100\mu s$
t_5	PP	Response to ATN+EOI	$\leq$ 200ns
T_6	C	Parallel Poll Execution Time	$\geq 2\mu s$
T_7	C	Controller Delay to Allow Current Talker to see ATN Message	$\geq$ 500ns
T_8	C	Length of IFC or REN False	$> 100\mu s$
T_9	C	Delay for EOI**	$\geq 1.5\mu s$††

* Time values specified by a lower case t indicate the maximum time allowed to make a state transition. Time values specified by an upper case T indicate the minimum time that a function must remain in a state before exiting.

† If three-state drivers are used on the DIO, DAV, and EOI lines, T_1 may be:
1. $\geq$ 1100ns
2. Or $\geq$ 700ns if it is known that within the controller ATN is driven by a three-state driver.
3. Or $\geq$ 500ns for all subsequent bytes following the first sent after each false transition of ATN (the first byte must be sent in accordance with (1) or (2).
4. Or $\geq$ 350ns for all subsequent bytes following the first sent after each false transition of ATN under conditions specified in Section 5.2.3 and warning note. See IEEE Standard 488.

‡ Time required for interface functions to accept, not necessarily respond to interface messages.

δ Implementation independent.

** Delay required for EOI, NDAC, and NRFD signal lines to indicate valid states.

†† $\geq$ 600ns for three-state drivers.

Appendix C
THE THREE WIRE HANDSHAKE

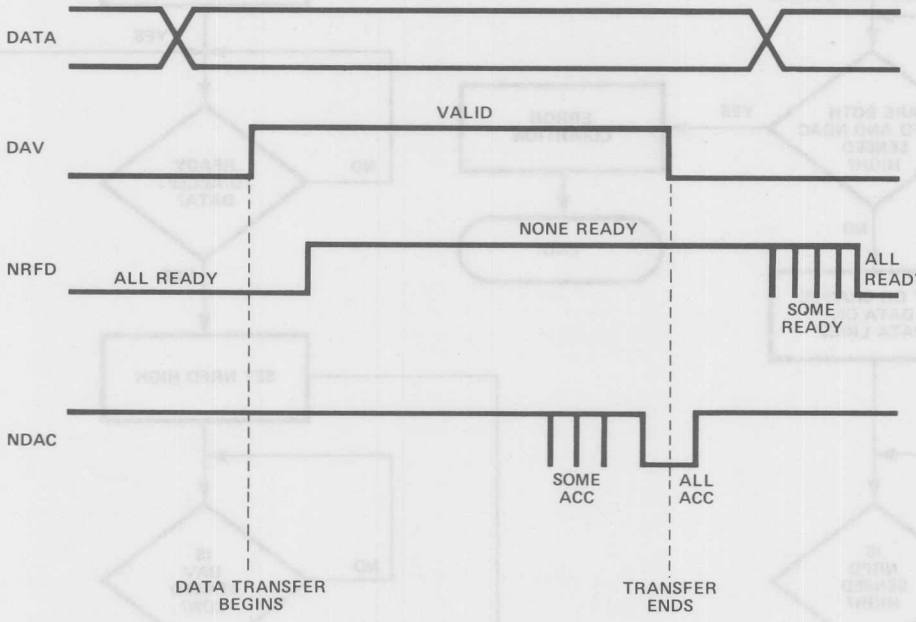
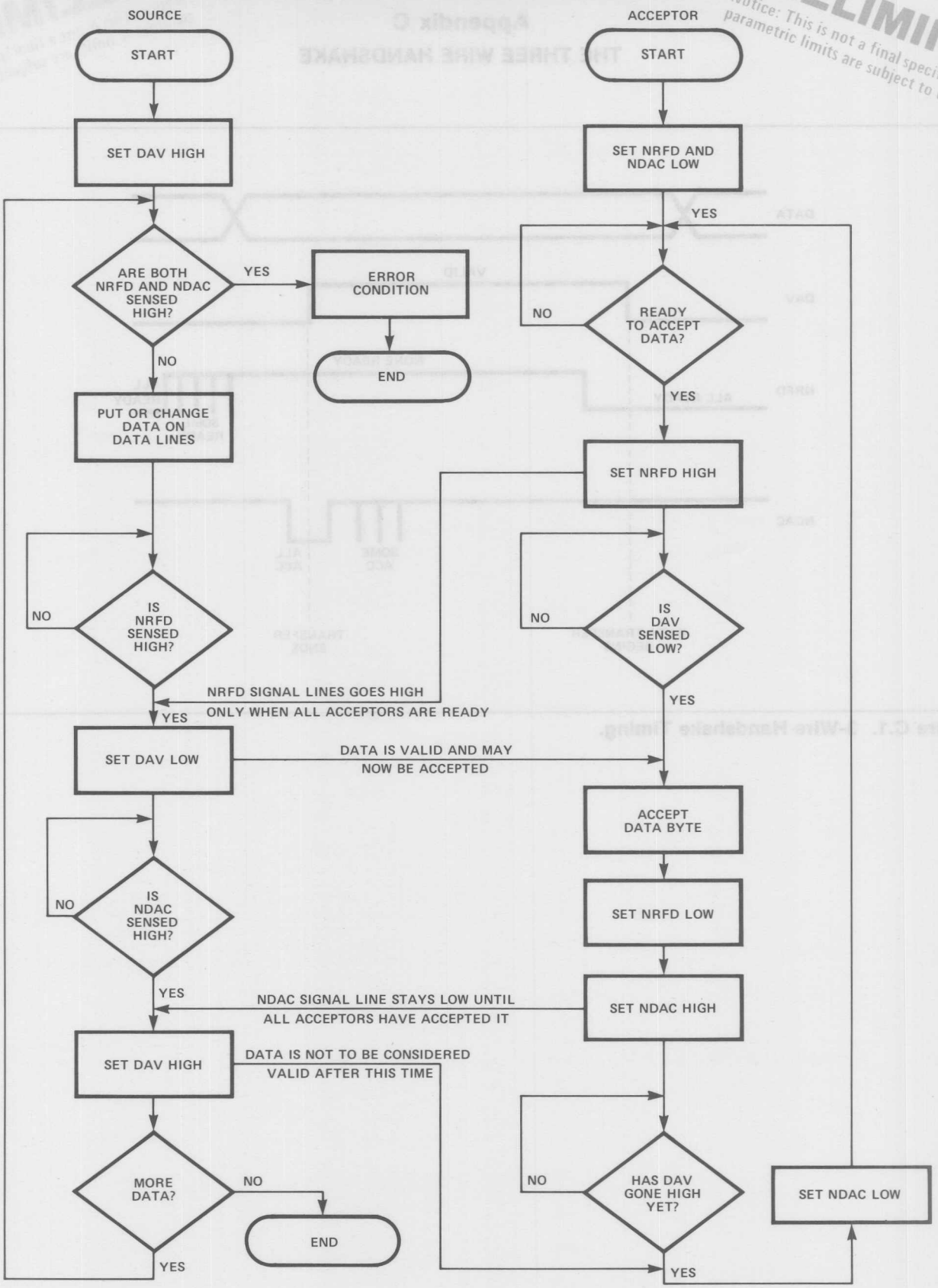


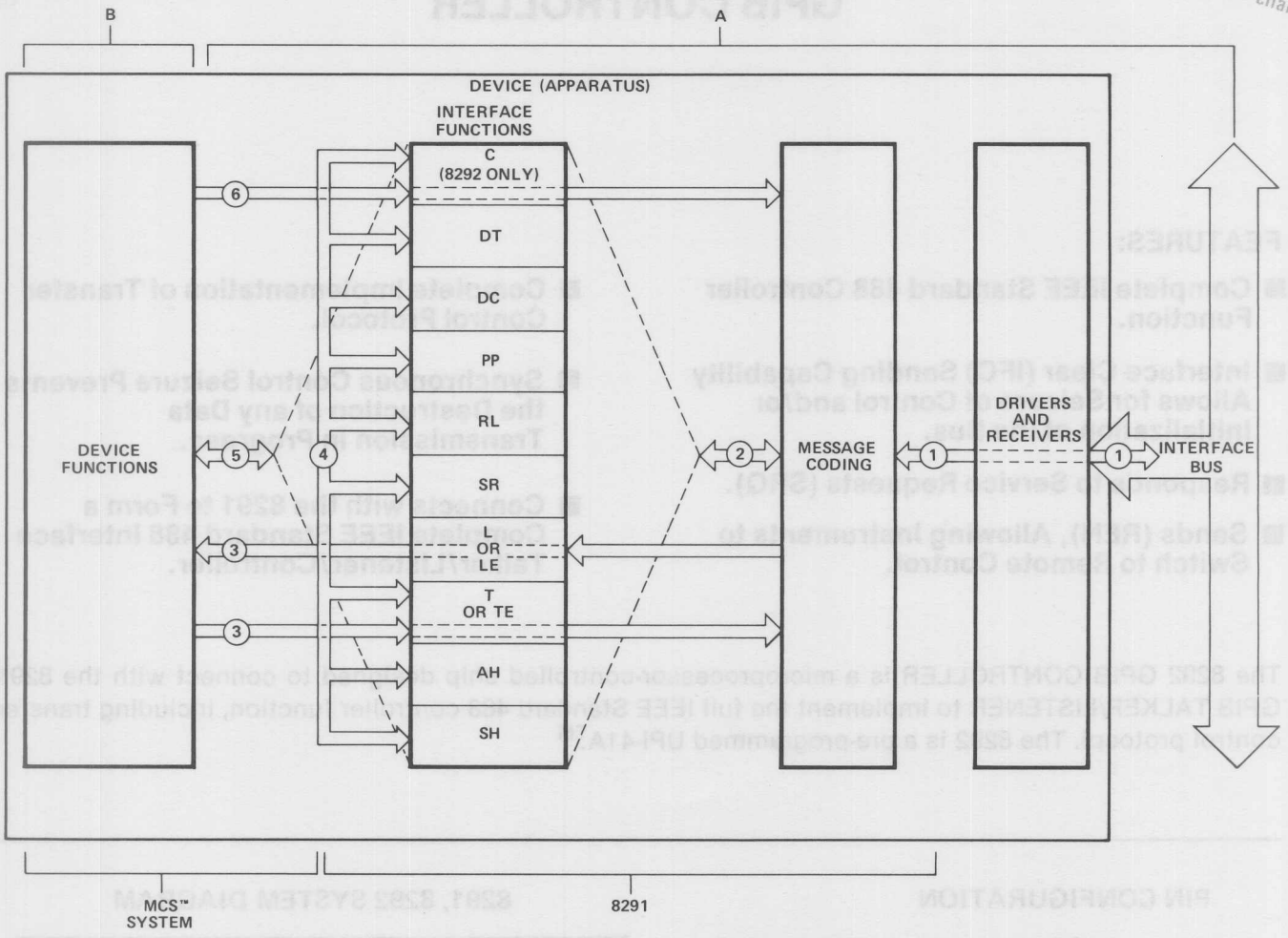
Figure C.1. 3-Wire Handshake Timing.



FLOW DIAGRAM OUTLINES SEQUENCE OF EVENTS DURING TRANSFER OF DATA BYTE. MORE THAN ONE LISTENER AT A TIME CAN ACCEPT DATA BECAUSE OF LOGICAL AND CONNECTION OF NRFD AND NDAC LINES.

Figure C.2. Handshake Flowchart.

Appendix D
FUNCTIONAL PARTITIONS



A – CAPABILITY DEFINED BY THE 488-1975 STANDARD.
B – CAPABILITY DEFINED BY THE DESIGNER.
1 – INTERFACE BUS SIGNAL LINES.
2 – REMOTE INTERFACE MESSAGES TO AND FROM INTERFACE FUNCTIONS.
3 – DEVICE DEPENDENT MESSAGES TO AND FROM DEVICE FUNCTIONS.
4 – STATE LINKAGES BETWEEN INTERFACE FUNCTIONS.
5 – LOCAL MESSAGES BETWEEN DEVICE FUNCTIONS AND INTERFACE FUNCTIONS (MESSAGES TO INTERFACE FUNCTIONS ARE DEFINED, MESSAGES FROM INTERFACE FUNCTIONS EXIST ACCORDING TO THE DESIGNER'S CHOICE).
6 – CONTROL MESSAGES (8292 ONLY).

Figure D.1. Functional Partition Within a Device.

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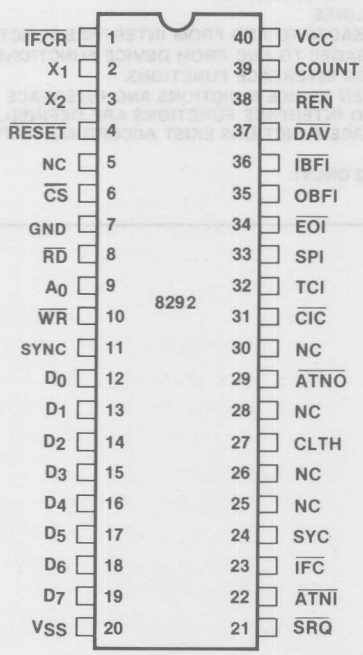
8292
GPIB CONTROLLER

FEATURES:

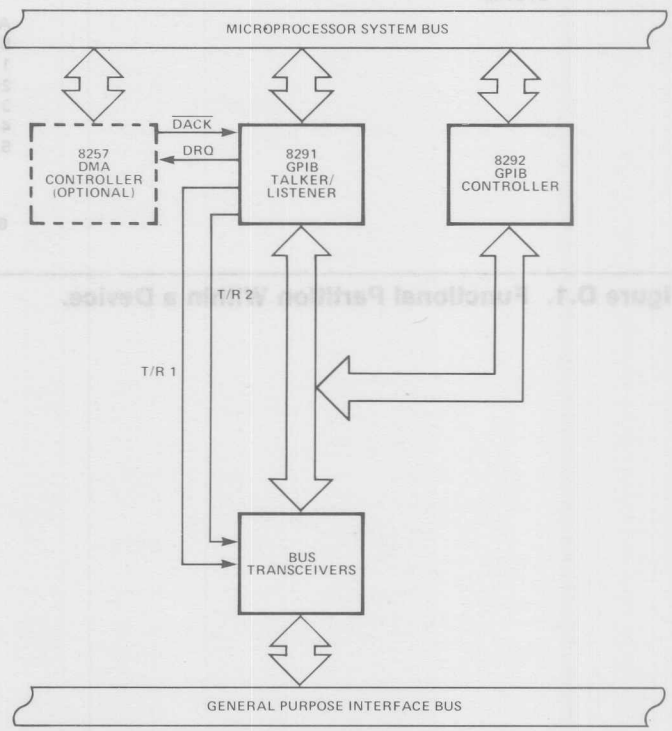
- Complete IEEE Standard 488 Controller Function.
- Interface Clear (IFC) Sending Capability Allows for Seizure of Control and/or Initialization of the Bus.
- Responds to Service Requests (SRQ).
- Sends (REN), Allowing Instruments to Switch to Remote Control.
- Complete Implementation of Transfer Control Protocol.
- Synchronous Control Seizure Prevents the Destruction of any Data Transmission in Progress.
- Connects with the 8291 to Form a Complete IEEE Standard 488 Interface Talker/Listener/Controller.

The 8292 GPIB CONTROLLER is a microprocessor-controlled chip designed to connect with the 8291 GPIB TALKER/LISTENER to implement the full IEEE Standard 488 controller function, including transfer control protocol. The 8292 is a pre-programmed UPI-41A.™

PIN CONFIGURATION



8291, 8292 SYSTEM DIAGRAM



PIN DESCRIPTION

Symbol	I/O	Pin No.	Function
D_0-D_7	I/O	12-19	8 bidirectional lines used for communication between the central processor and the 8292's data bus buffers and status register.
A_0	I	9	Address Line—Used to select between the data bus and the status register during read operations and to distinguish between data and commands written into the 8292 during write operations.
$\overline{CS}$	I	6	Chip Select Input—Used to select the 8292 from other devices on the common data bus.
$\overline{RD}$	I	8	I/O write input which allows the master CPU to write to the 8292.
$\overline{WR}$	I	10	I/O read input which allows the master CPU to read from the 8292.
$\overline{RESET}$	I	4	Used to initialize the chip to a known state during power on.
$\overline{DAV}$	I/O	37	DAV Handshake Line—Used only during parallel poll, configures to force the 8291 to accept the parallel poll status bits.
$\overline{ATNI}$	I	22	Attention In—Used by the 8292 to monitor the GPIB ATN control line. It is used during "take control synchronously" execution and during the transfer control procedure.
$\overline{CIC}$	O	31	Controller In Charge—Controls the S/R input of the SRQ bus transceiver. It can also be used to indicate that the 8292 is in charge of the bus.
$\overline{EOI}$	I/O	34	End Or Identify—One of the GPIB management lines, as defined by IEEE Std. 488-1975. Used with ATN as Identify Message during parallel poll.
$\overline{IFC}$	I/O	23	Interface Clear—One of the GPIB management lines, as defined by IEEE Std. 488-1975, places all devices in a known quiescent state.
SYC	I	24	System Controller—Monitors the system controller switch.
OBFI	O	35	Output Buffer Full—Used as an interrupt to the central processor while the output buffer of the 8292 is full. The feature can be enabled and disabled by the interrupt mask register.
$\overline{IBFI}$	O	36	Input Buffer Not Full—Used to interrupt the central processor while the input buffer of the 8292 is empty. This feature is enabled and disabled by the interrupt mask register.
$\overline{ATNO}$	O	29	Attention Out—Controls the ATN control line of the bus through external logic for tcs (take control synchronously) purpose. (ATN is a GPIB control line, as defined by IEEE Std. 488-1975.)
$\overline{SRQ}$	I	21	Service Request—One of the IEEE control lines. Sampled by the 8292 when it is controller in charge, if true—SPI interrupt to the monitor will be generated.
$\overline{REN}$	O	38	The Remote Enable bus signal selects remote or local control of the device on the bus. A GPIB bus management line, as defined by IEEE Std. 488-1975.
TCI	O	32	Task Complete Interrupt—Interrupt to the control processor used to indicate that the task requested was completed by the 8292 and the information requested is ready in the data bus.
SPI	O	33	Special Interrupt—Used as an interrupt on events not initiated by the central processor.
CLTH	O	27	CLEAR LATCH Output—Used to clear the $\overline{IFCR}$ after recognized by the 8292. Usually low (except after hardware Reset), will be pulsed low when $\overline{IFCR}$ is recognized by the 8292.
$\overline{IFCR}$	I	1	IFC Received (latched)—The 8292 monitors the IFC Line (when not system controller) through this pin.
COUNT	I	39	Count Input—When enabled by the proper command the internal counter will count external events through this pin. High to low transition will increment the internal counter by one. The pin is sampled once per three internal instruction cycles (7.5 μsec when using 6 MHz XTAL). It can be used for byte counting when connected to NDAC line, or for block counting when connected to the EOI line.
X_1,X_2	I	2,3	Inputs for a crystal, LC or an external timing signal to determine the internal oscillator frequency.
SYNC	O	11	8041A instruction cycle synchronization signal; it is an output clock with a frequency of XTAL ÷ 15.
V_{CC}	P.S.	40	+5V supply input.
V_{SS}	P.S.	7,20	Circuit ground potential.

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